Electrostatic Simulations for Two-Dimensional Semiconductor-Superconductor Hybrid Devices

Bachelor's thesis

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Abstract

In this thesis we study the electrostatics of recently investigated two dimensional semiconductor-superconductor hybrid devices, that host Majorana Zero Modes (MZMs) [Fornieri et al., 2019],[Nichele et al., 2017]. We conduct electrostatic simulations using COMSOL multiphysics, and solve a three dimensional Thomas-Fermi model using the finite element method.

In our work, we have successfully recreated experimental data from three recently investigated devices, by reproducing qualitative features of experimental conductance gate-gate maps. The devices are based on InAs/InGaAs quantum wells realized in planar heterostructures, in contact with a superconducting layer [Shabani et al., 2016].

We have verified experimental intuition regarding the geometry of the devices, and how this affects tunneling spectroscopy in the devices. We focus on the electrostatic potential generated by quantum point contacts (QPC's), formed by two negatively biased split gates, placed at the edge between a superconducting and a non-superconducting region. We show that when the QPCs are in proximity of another grounded gate at 0V, it is possible to define a sharp tunnel barrier that can be used to perform effective tunneling spectroscopy.

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CHAPTER 1

Introduction

1.1 Intro

Topological superconductivity is a state of matter associated with Majorana zero modes (MZMs) [Leijnse and Flensberg, 2012]. Because of their non-abelian exchange properties, and their non-local nature, MZMs are ideal candidates for low-decoherence topological quantum computation. In the last 7 years, a great experimental effort by several groups in the world has brought evidence supporting the existence of MZMs in hybrid superconductor/semiconductor heterostructures [Lutchyn et al., 2017]. MZM's appear as zero energy states in the middle of the superconducting gap and they can be experimentally probed by means of tunneling spectroscopy.

In this thesis, we examine the electrostatic properties of two-dimensional superconductor-semiconductor hybrid devices, which can host MZMs. Our simulations are based on a 3D Thomas-Fermi Model, which is solved with the finite element method. The goal is to study specific device designs, and compare these to experimental data from the same devices. This will allow us to characterize spectroscopic properties of the devices, and verify experimental intuition regarding the effects of different geometries on the electrostatics of the devices.

1.2 Two Dimensional Electron Gas Heterostructures

The devices we are simulating are fabricated in planar heterostructures. By using the method of band gap engineering, a quantum well is created in a layer of the heterostructure. This confines the electrons to move in two dimensions and they form a two dimensional electron gas (2DEG), as shown in figures 1.1 a) and b). The heterostructures used in our simulations are based on epitaxially grown InAs/InGaAs quantum wells. An illustration of the heterostructure is shown in figure 1.1 a). In this setup, the electrons are confined in the InAs layer, that is separated by a topbarrier of InGaAs from the superconductor to increase electron mobility [Shabani et al., 2016]. The epitaxial aluminum is etched onto the 2DEG, and Ti/Au gates are evaporated onto the top of the structure. The gates are separated from the 2DEG by 15 nm of insulating HfO_2. These systems achieve flat, abrupt and impurity free interfaces, and can be used to create superconductor-semiconductor devices that are easily gateable and support topological superconductivity [Shabani et al., 2016].

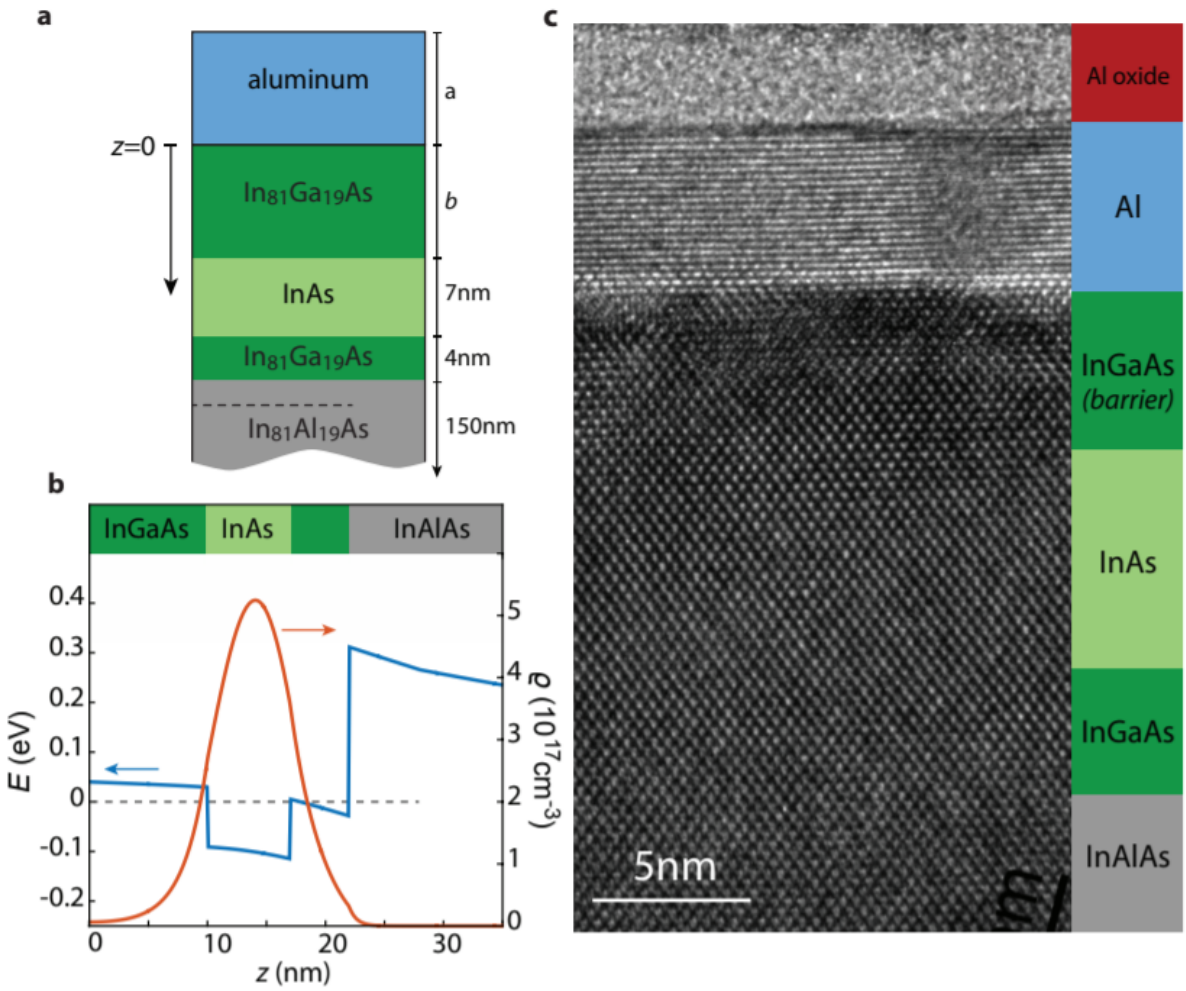

Figure 1.1: InAs/InGaAs quantum well structure, a) is a schematic view of the structure, b) is an illustration of the energy, created by a self consistent Poisson solver, blue is the energy band gap, and red is the electron wave function. c) shows a TEM micrograph of the structure. Figure from [Kjaergaard, 2015] PhD Thesis, p. 11.

A useful property of 2DEG's is that the density of states is independent of energy.([Ihn, 2010] p. 70)

$$D_{2DEG} = \frac{m*}{2\pi\hbar^2} \tag{1.1}$$

This is useful firstly because it simplifies many equations, and secondly because it allows us to probe the density of states in the hybrid devices without having to worry about energy dependence in the 2DEG lead. This is particularly helpful when performing tunneling spectroscopy.

1.3 Tunneling Spectroscopy

Tunneling spectroscopy is a method used to probe the density of states of a conducting sample. This is achieved by placing a potential barrier between the sample and an electron reservoir, so that electronic transport through the system is caused only by quantum tunneling. A common way to do this is using a conducting needle, which is placed very close to the surface of a conductor. It is then possible to use the vacuum between the needle tip and the surface as a tunneling barrier. By applying a voltage

to the needle and adjusting the distance to the surface, tunneling transport can be achieved.

Instead of a vacuum barrier, we use a QPC to constrict the electron transport in a 2DEG, with electron reservoirs on either side of the QPC. One reservoir is defined in the 2DEG, beneath a grounded helper gate that screens the electrostatic potential generated by the QPCs. The other reservoir is near the superconductor-semiconductor interface. This region is expected to host MZMs and represents the area of interest where we want to perform tunneling spectroscopy. By applying a negative voltage to the QPC gates, we can create a potential barrier and measure current flowing through the QPC (see eq. 1.2). In order to obtain high energy resolution in spectroscopy, this barrier must be sharp and narrow, allowing that electron transport occurs only by means of quantum tunneling, and avoiding the formation of unintended quantum dots. This is explored further in section 2.3

The tunneling current is written in eq. 1.2 ([Ihn, 2010] p. 199), where T is the transmission probability, $D_{L,R}$ are the densities of states of the left or right reservoirs and f is the Fermi distribution function. If one of the densities of states and the tunneling probability are independent of energy, it is possible to probe the remaining density of states.

$$I = -\frac{(2\pi)^2|e|}{h}\int dE\ T\ D_L(E)D_R(E)[f_L(E) - f_R(E)] \tag{1.2}$$

1.4 Superconductivity

In our work we have focused on two different superconductor-semiconductor hybrid devices, which have been experimentally investigated to study topological superconductivity [Nichele et al., 2017], [Suominen et al., 2017], [Fornieri et al., 2019].

Superconductivity is a phenomenon where a metal conducts electricity without electrical resistance. To explain this phenomenon, the Bardeen-Cooper-Schrieffer theory introduces Cooper pairs of electrons, where 2 electrons with opposite wave vector and spin ($\mathbf{k}\downarrow, -\mathbf{k}\uparrow$) condensate into a superconducting state. This opens an energy gap (Δ) between the ground state of Cooper pairs and excited quasiparticle states [Bardeen et al., 1957]. Because of this energy gap, scattering processes are suppressed, which vanishes the electrical resistance of the conductor.

An interesting phenomenon of superconductors is that the superconducting properties "leak" into materials near a superconducting junction. If we imagine a superconductor-normal (SN) interface, the normal metal will exhibit superconducting properties, like a dissipationless supercurrent and a reduced density of states, near the junction. This is called the proximity effect. The Cooper pairs from the superconductor transfer into the normal metal, where they will diffuse a certain distance before they decay ([Schäpers, 2001] p. 14). This decay takes place on a length scale given by the coherence length.

The first device we have simulated is a Josephson junction (JJ), consisting of a superconductor-normal-superconductor interface, that allows proximity induced superconducting transport through the normal part of the junction. In this device a QPC is placed at the top end of the junction, this can be used for tunneling spectroscopy to probe the density of states in the junction.

It has been predicted that this system could host topological superconductivity ([Pientka et al., 2017], [Hell et al., 2017]). Recently, experimental evidence consistent with these predictions has been reported [Fornieri et al., 2019], [Ren et al., 2019]

The secondary device we have simulated is a quasi 1D hybrid structure, with a QPC at its end (NIS QPC), that has been used to investigate the properties of zero bias peaks in conductance, which were consistent with MZMs. [Nichele et al., 2017]

CHAPTER 2

Methods

2.1 Thomas Fermi Approximation

The Thomas-Fermi approximation is a semi-classical approximation that gives a quantum mechanical model for the electronic structure of many body systems. The essence of the model is that the total kinetic energy (T) of the electrons, can be expressed by the spatially varying electron density (n), as expressed in eq. 2.1 (in three dimensions) [Virginia Tech, 2013]

$$T = C \int [n(r)]^{5/3} d^3 r \tag{2.1}$$

The Thomas-Fermi approximation now gives us a way to calculate the density, by assuming a non-interacting uniform electron gas. We start by writing up the relation between the Fermi momentum and the density of a 2DEG:

$$n(r) = \frac{k_f^2}{2\pi} \tag{2.2}$$

We then approximate the kinetic energy using the Thomas-Fermi functional:

$$T[n] = \int d^3 r \frac{3}{5} \frac{\hbar^2 k_f^2(r)}{2m*} n(r) \tag{2.3}$$

If we then minimize the total energy with respect to the density, with the constraint of a constant electron number, we get:

$$\delta(T + \int n(r) V(r) d^3 r - \mu \int n(r) d^3 r)/\delta n = 0 \tag{2.4}$$

Solving this equation gives the following expression for the chemical potential (μ):

$$\mu = \frac{\hbar^2 k_f^2(r)}{2m} + V(r) \tag{2.5}$$

This approximation is valid if the variations of the external potential are weak in the scale of the Fermi wavelength.

If we then combine equation 2.2 and 2.5, we can find an expression for the density:

$$\mu = \frac{\hbar^2 n(r) 2\pi}{2m*} + V(r) \tag{2.6}$$

$$n(r) = \frac{m*}{\pi \hbar^2} (\mu - V(r)) \tag{2.7}$$

The advantage of the Thomas-Fermi approximation is that it allows us to solve a complex quantum mechanical problem, without the need for solving the Schrödinger equation.

2.2 COMSOL Multiphysics(FEA)

The simulations are performed with a software called COMSOL multiphysics. The software gives the user the ability to create a desired geometry, and apply properties such as electrostatics, temperature, or stress/strain to individual parts of the geometry. The software can then use finite element analysis (FEA) to simulate how the device will behave to specified inputs. This method breaks the simulation into smaller parts of a geometry, and applies rigorous boundary conditions and test functions to get accurate results. This method is explained in detail in appendix A.1.

2.2.1 COMSOL Electrostatics

In this thesis we will focus only on the electrostatic properties of the gates defining the devices. For a static electrical field, Maxwell's equations simplify to the following partial differential equations[COMSOL, 2015].

$$\nabla \cdot \mathbf{D} = \rho \tag{2.8}$$

$$\mathbf{D} = \varepsilon_0 \varepsilon_r \mathbf{E} = \varepsilon_0 \mathbf{E} + \mathbf{P} \tag{2.9}$$

$$\nabla \times \mathbf{E} = 0 \tag{2.10}$$

Here $\mathbf{D}$ is the electric displacement field, $\mathbf{E}$ is the electric field, and $\mathbf{P}$ is the polarization density. ε_0 and ε_r are the vacuum permittivity and the relative permittivity respectively. In equation 2.8 we have Gauss' law, and in equation 2.10 we have Faraday's law for a static electrical field. From Faraday's law we can express the electrical field as a function of the electrical potential $\mathbf{E} = -\nabla V$. This can be put into Gauss' law, so we have the following equation. [COMSOL, 2015]

$$-\nabla \cdot (\varepsilon_0 \nabla V - \mathbf{P}) = \rho \tag{2.11}$$

In this work, we are using the electrostatics interface, and therefore are running stationary simulations. This means that the charges do not have time to redistribute (as no time passes during the simulations), thereby we have that the charge distribution can be considered as a given input for the model [COMSOL, 2015]. Under this condition, the approach is to solve for the electrostatic configuration by using the electric potential V. As shown in the formulation of Gauss' law in eq. 2.11, we now have a variant of the Poisson equation for the electrical potential, which is solved within the electrostatics interface of the AC/DC module in COMSOL [COMSOL, 2015]. At an interface between two materials, we have following boundary condition:

$$\mathbf{n_2} \cdot (\mathbf{D_1} - \mathbf{D_2}) = \rho_s, \tag{2.12}$$

Where $\mathbf{n_2}$ is the unit vector normal to the interface pointing into material 1, while ρ_s is the surface charge density. In the absence of surface charges this equation turns into the natural boundary condition[COMSOL, 2015].

We use COMSOL to create our device geometry, define the electrostatics of the different layers of the heterostructure, and then simulate the effect of specific voltages applied to the desired gates. This gives us the ability to explore the pinch-off properties of different geometric designs.

We define an electrical potential for each of the gates, and a surface charge density at the 2DEG plane. We use the Thomas-Fermi approximation (eq. 2.7) for a 2DEG to create a model for the surface charge density with 2 parameters: the chemical potential, and a free parameter called V_0. Since there is not enough experimental evidence to determine V_0, we treat it as a free parameter. A physical interpretation of V_0 could be the difference from the aluminum work function and the top of semiconductor stack, but it is beyond the scope of this project to investigate this further. We use the potential $V(r) = V_0 - eV$

$$n_{2DEG} = \frac{m*}{\pi\hbar^2}(E_f - (V_0 - eV))\theta[E_f - (V_0 - eV)] \tag{2.13}$$

This gives us a relation between the electric potential and the electron density, without the need to solve the Schrödinger equation. To make the model more accurate, we also include a term that accounts for the electrostatics caused by the semiconductor-insulator interface. This is called the density of interface traps (DIT) term, and is show in eq 2.14

$$n_{DIT} = -eD_{IT}(E_f - (E_0 - eV)) \tag{2.14}$$

This introduces two new parameters, the DIT constant: D_{IT}, and the neutral level: E_0. The DIT constant is a measure of how clean the interface is, and the neutral level is a free parameter.

2.3 Device Designs

We have simulated two separate device design, and four different devices. We have two Josephson junctions, one with a protrusion at the edge of the helper Gate, and one without. We also have two normal-insulating-superconductor (NIS) devices, one with a protrusion and one without. The design and purpose of the protrusion is explained in the following section. We have experimental data for three of these devices: both Josephson junctions, and the NIS device with the protrusion.

2.3.1 Josephson Junction Device

The first device we have simulated is a Josephson junction (see section 1.4), with a QPC at the top end for spectroscopy purposes. The device consist of a Josephson junction with a gate (called the wire gate) on top of the semiconductor gap between the superconducting aluminum forming the junction. This device has a QPC coupled to the top end of the junction, and a helper gate to control the electron

density in the 2DEG. An illustration of the setup is shown in figure 2.1.

We expect electronic transport through the bottom of the helper gate, down through the junction, and we can control this transport by applying a negative voltage to the QPC gates. This negative voltage will create a potential barrier at the end of wire, and at negative enough V_{qpc} the transport will be completely stopped. At this point the transport is "pinched off".

The wire gate and the helper gate is used to screen the electrons in the 2DEG from the electric potential from the QPC, by keeping these gates grounded. This helps in creating a sharp tunnel barrier near the QPC. If we apply a negative voltage to the helper gate, it also pinches off the transport at some point, as we deplete the electrons below the helper gate.

In our work we have variants of this design, one with a small protrusion on the edge of the helper gate, that is used to create a sharper tunneling barrier, and one without a protrusion. Because of the enhanced potential barrier the protrusion provides, it can be used effectively to probe the density of states in the Josephson junction. [Fornieri et al., 2019]. A schematic overview of the device is shown in figure 2.1.

We have experimental data both with and without the protrusion, and we will therefore be able to compare the simulations with the data, in both cases.

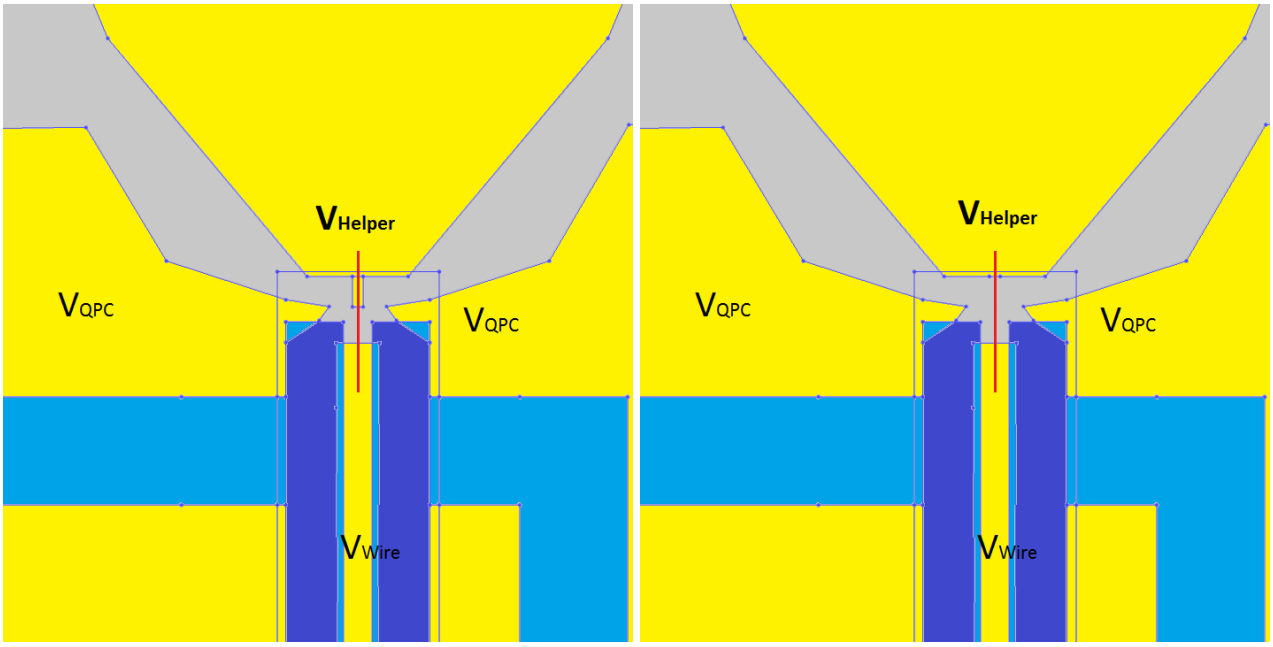

Figure 2.1: Schematic overview of the Josephson junction device. The left is the design with the protrusion, the right is the design without the protrusion. The grey area is the 2DEG, the blue is the aluminum superconductor and the yellow is the Ti/Au gates. The teal area is where the gates overlap with the aluminum. The red line represents the cut along which we calculate the electron density for figures 3.7 and 3.8

2.3.2 NIS QPC Device

The second kind of devices we have been focused on is a normal-insulator-superconductor quantum point contact coupled to an aluminum wire, with a wire gate and a helper gate to control the electron density in the 2DEG. An illustration of the setup is shown in figure 2.2. As with the Josephson junction devices, we expect electron transport through the top of the wire (below the helper gate) down through the superconductor (aluminum), and we can control this transport by applying a negative voltage to the QPC gates, in the same fashion as the JJ Device.

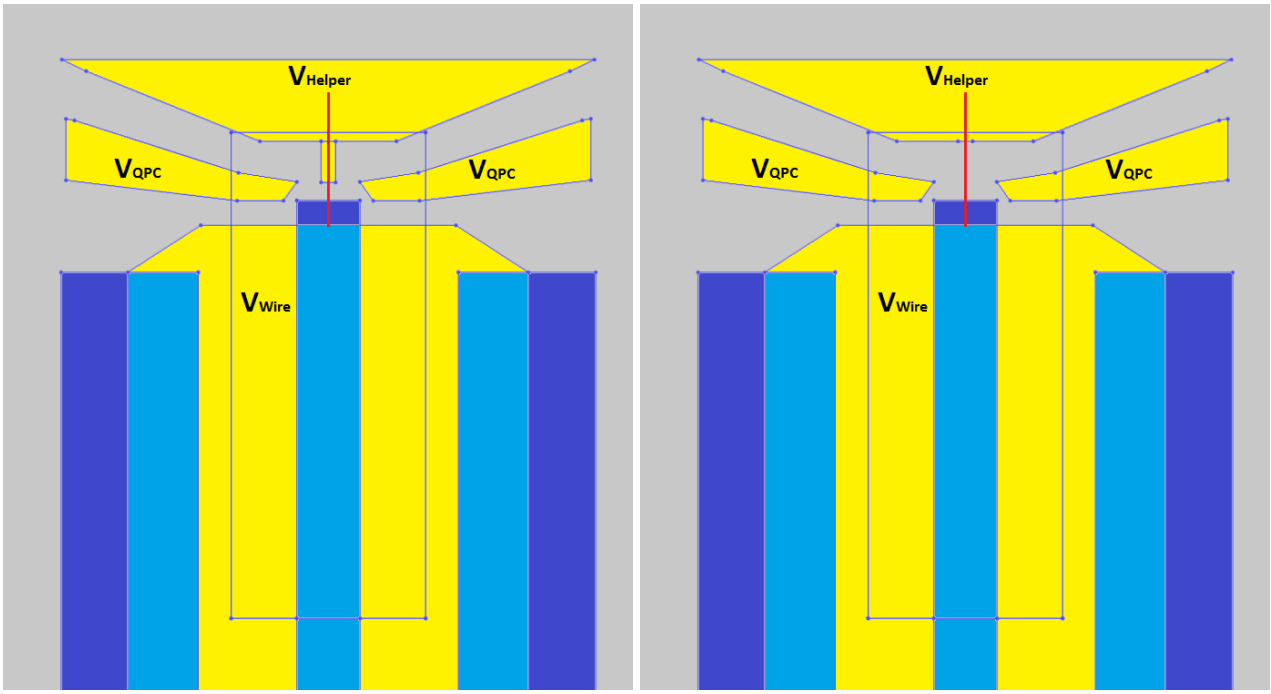

Figure 2.2: Schematic overview of the NIS Device. The left is the design with the protrusion, the right is the design without the protrusion. The grey area is the 2DEG, the blue is the aluminum superconductor and the yellow is the Ti/Au gates. The teal area is where the gates overlap with the aluminum. The red line represents the cut along which we calculate the electron density for figures 3.14 and 3.15

Making a proper simulation of the electrons in this quantum mechanical tunneling regime is beyond the scope of this project. It requires an accurate 3 dimensional Schrödinger-Poisson solver, which would require further work. What is possible however, is to calculate the carrier density using approximations, and evaluate the effect of the protrusion on the electrostatics, by comparing simulations with experimental data from other similar devices.

CHAPTER 3

Results and Discussion

3.1 Parameter Fitting

Now our model contains 3 free parameters, The DIT constant, E_0 and V_0 (equation 2.13 and 2.14). The DIT constant was determined to be $D_{IT} = 10^{11} eV^{-1} cm^{-2}$, by using Hall bar measurements of the same wafer that was used for our NIS device. This constant should transfer directly to our device as well, because the fabrication process is identical. From the same data, E_0 was set to 0.

We then used the pinch-off data from the device to fit V_0. We knew the pinch off voltage, and varied V_0 until our simulations matched the experimental results (shown in figure 3.1). We did this for the devices with the protrusion, and used the parameters for the devices without protrusions as well.

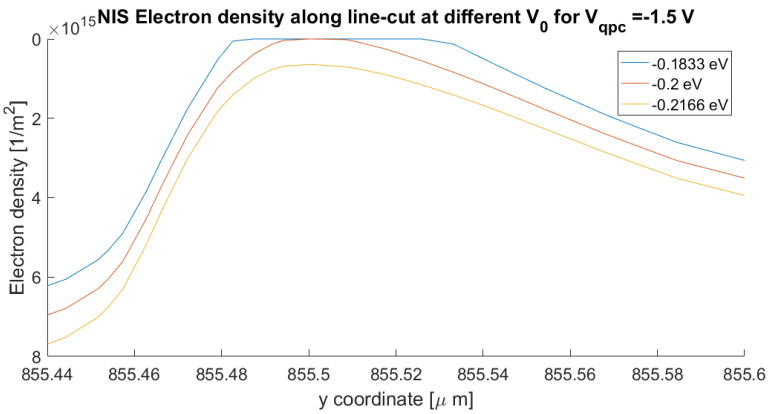

Figure 3.1: Plot showing the electron density along a line-cut in the middle of the NIS wire channel for the three most relevant values of V_0, as explained in section 3.1. We set the QPC gate voltage to the pinch off voltage ($V_{QPC} = -1.5V$), and varied the voltage offset V_0 in an appropriate range. We then chose the smallest offset that still produced pinch-off at the correct voltage. For the NIS Device, this value is $V_0 = 0.2eV$, as this is the electronic density is zero at one or more points along the line-cut.

In order to test our model, we compare the calculated electron density along the red lines shown in figure 2.1 and 2.2, to the experimental conductance maps measured as a function of V_{qpc} and V_{helper}, called gate-gate maps.

For the gate-gate maps, we used the minimum electron density on a vertical line-cut in the middle of the QPC, extending into the part below the helper gate protrusion (shown as a red line in figure 2.2

and 2.1). Using a line-cut allows us to get an informative picture of the density in the QPC channel, and makes it easier to compare our simulations to the experimental data. When comparing the simulations to experimental data, we interpret the conductance to be 0 if there is a point along the specified line that is depleted of electrons (a point with 0 carrier density).

The data gathered on the devices are used to create pinch-off plots and gate-gate maps. The pinch off plots are, traditionally, plots of conductance as a function of QPC voltage. Conductance is measured in units of $G_0 = \frac{2e^2}{h}$, called the conductance quantum ([Ihn, 2010] pp. 177-182).

As a consequence of using the electron density, we can only get meaningful comparisons to the experimental data along the boundary defined by the pinch off voltage for each V_{helper} value in the gate-gate maps. The effect of this is also that the actual value of the electron density at a specific gate voltage combination is not strictly comparable to the conductance, as we do not know the direct relation between the electron density and conductance. This is important to keep in mind when comparing the data from our gate-gate map simulations with the experimental data.

3.2 2D Density Maps, Pinch Off Plots, and Gate-Gate Maps

3.2.1 Josephson Junction Devices

In the following section, we show 2D maps of the electron density, in the plane of the 2DEG. These maps help to visualize the effect of the different geometries on the carrier density in the 2DEG. Figures 3.2, 3.3, 3.4 show the Josephson junctions.

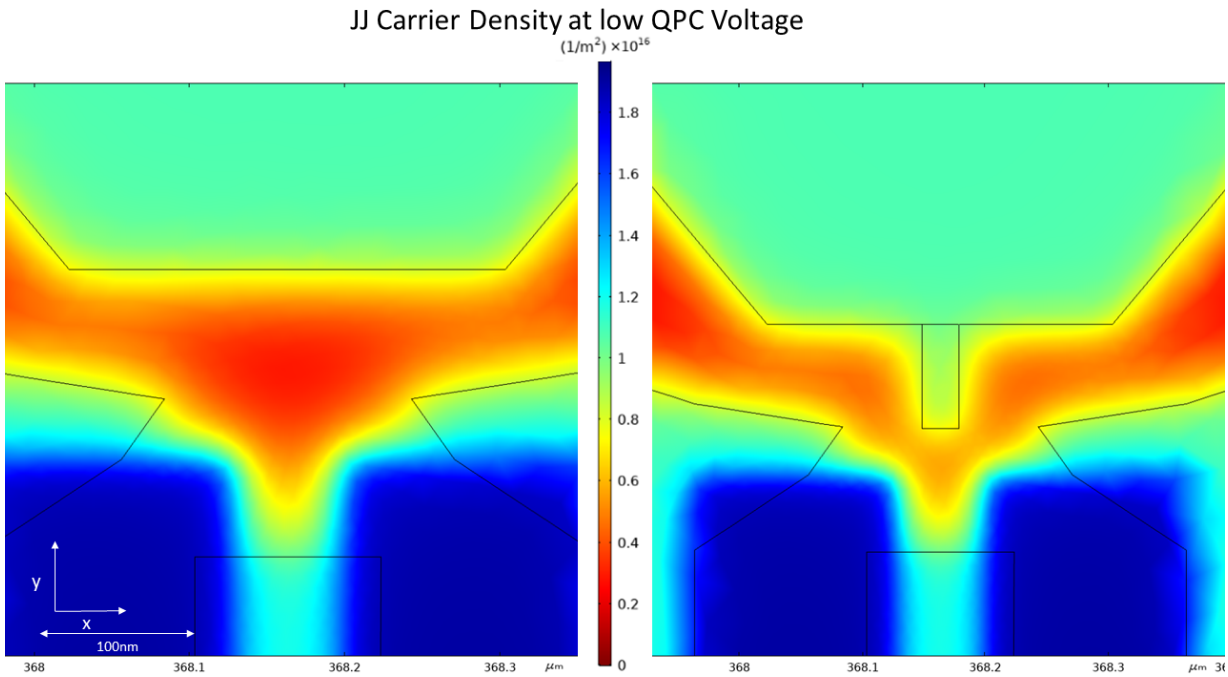

Figure 3.2: 2D maps of electron density at the surface of the 2DEG. For the right we have the device with the protrusion, and for the left we have the device without the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = 0V$. We consider this a low QPC voltage for both devices, in relation to the pinch off voltage

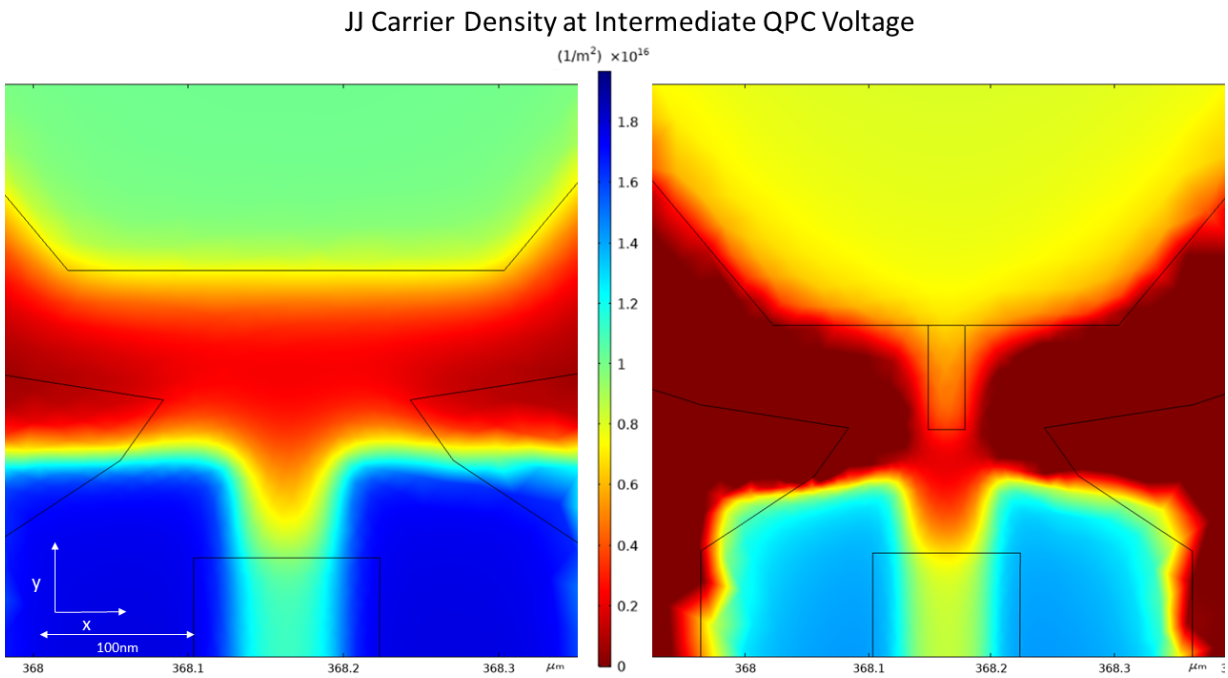

Figure 3.3: 2D maps of electron density at the surface of the 2DEG. For the right we have the device with the protrusion, and for the left we have the device without the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = -1.71V$ for the right figure, and $V_{helper} = 0V$ and $V_{QPC} = -0.45V$ for the left figure. We consider this a intermediate QPC voltage for both devices, in relation to the pinch of voltage

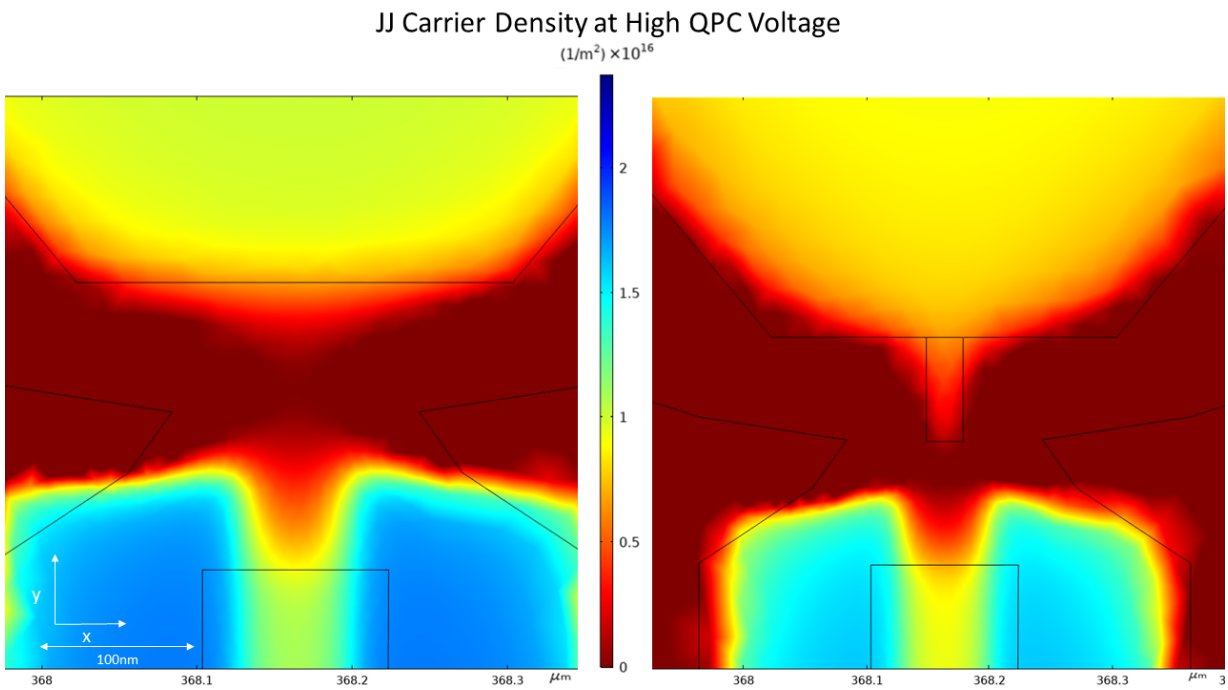

Figure 3.4: 2D maps of electron density at the surface of the 2DEG. For the right we have the device with the protrusion, and for the left we have the device without the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = -2.52V$ for the right figure, and $V_{helper} = 0V$ and $V_{QPC} = -1.35V$ for the left figure. We consider this a high QPC voltage for both devices, in relation to the pinch off voltage.

From figure 3.2 we see how the electron density in the 2DEG is distributed in the case where we set

all gates to $0V$. In this case we observe an open wire, with no pinch off. It should be noted that the electron density distribution below the aluminum, and the gates, is significantly higher than the rest of the 2DEG. This behavior is consistent with what we would expect because of the effect of V_0 (see section 2.2.1 for clarification).

As we increase the voltage on the QPC gates, see figure 3.3, it is apparent that for both devices, the area below the QPC gates is depleted. The density between the helper gate and the wire gate is lower than before, while it has yet to completely reach zero.

When we apply a higher voltage on the QPC gates, we see that the electron density between the wire and the helper gates reaches zero. The wire is therefore pinched off at this voltage. As we see in figure 3.4 this occurs at different QPC voltages. The map in figure 3.4 to the left and the map in figure 3.3 to the right are at approximately the same voltage. If we compare these two maps, it is clear to see the effect of the protrusion on the carrier density in the QPC channel.

Moreover, the width of the channel when close to the pinch off condition is significantly different in the case with the protrusion. With the protrusion, the width of the channel is approximately $180nm$, and without the protrusion, the width is approximately $300nm$. This is almost two times as large as with the protrusion.

These following plots clearly show the pinch off points of the devices. The pinch off plot from for the experimental Josephson junction device data is shown in figure 3.5, and the experimental NIS QPC data is shown in figure 3.13.

The gate-gate map from the Josephson junction device is shown in figure 3.7 and in figure 3.14 for the NIS QPC Device.

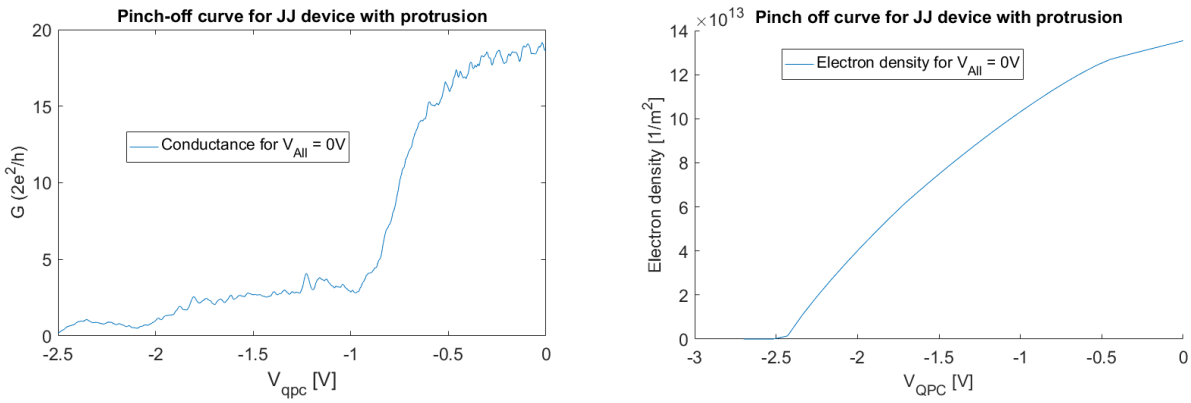

Figure 3.5: Pinch-off plot for the Josephson junction device with the protrusion. To the left we have the measured conductance and to the right we have the simulated electron density.

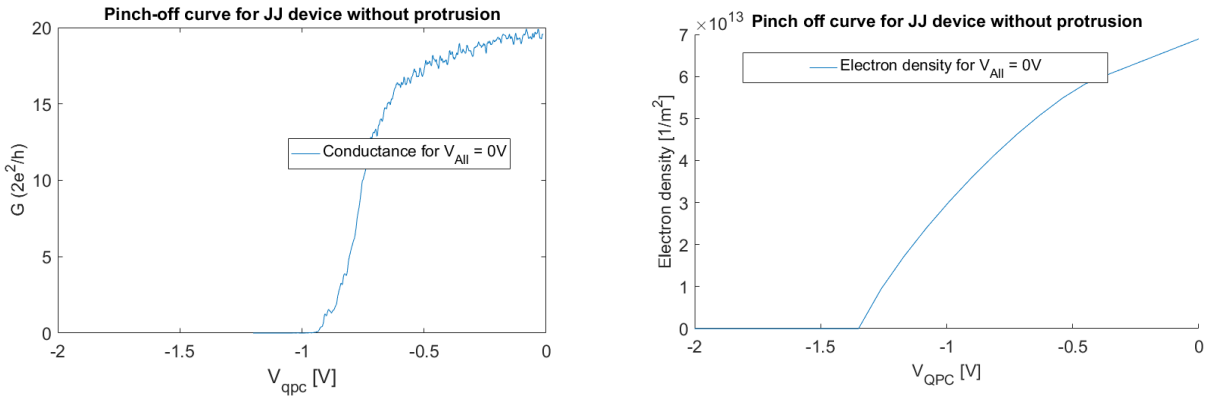

Figure 3.6: Pinch-off plot for the Josephson junction device without the protrusion. To the left we have the measured conductance and to the right we have the simulated electron density.

For the pinch off plots with the protrusion, the simulations are in agreement with the data. in figure 3.5, we can clearly see that the electron density and the conductance reach zero at the same QPC voltage, $V_{QPC} = -2.5V$. This is caused by our fitting process, since we fit V_0 using this exact voltage. The shapes of the pinch off curves are different, the conductance take a sharp drop from $V_{QPC} = -0.5V... - 1V$, and then decreases in a erratic, but almost linear fashion. This is because depletion happen in the sharp range, but the channel is not completely pinched off. In the calculated density curve, we see a almost steady decreasing parabola. This steady decrease is also expected, since the density is a spatially local phenomenon.

For the pinch off plots without the protrusion, it is clear that the data is not in agreement with the simulations. The pinch off in the simulations happen at $V_{QPC} = -1.2V$, whilst the pinch off from the experimental data is at about $V_{QPC} = -0.9V$. Our interpretation of this behavior is that depletion in the 2DEG happens more locally in the area below the gates than what we would expect, which coincides with the QPC gate pinching off at higher voltages, when there is no applied voltage on the helper gate.

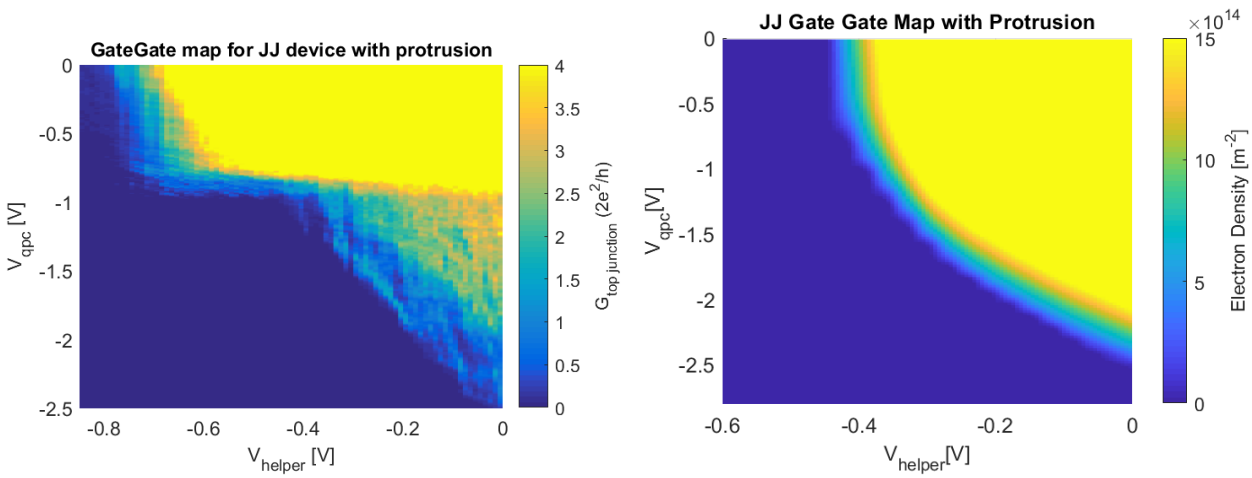

Figure 3.7: Gate-gate map of Josephson junction device. Left: with protrusion, right: without protrusion. On the left plot, the conductance tail is clearly visible as expected. The pinch off point is around $V_{QPC} = -2.5V$, which is in agreement with the pinch off data seen in figure 3.5.

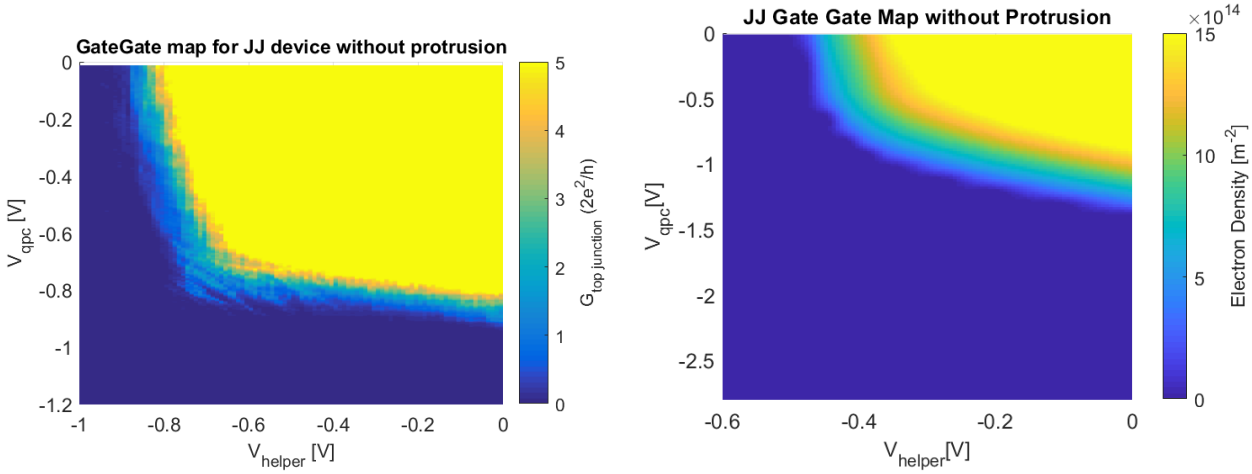

Figure 3.8: Josephson junction gate-gate map with protrusion(left) and without protrusion(right). The major difference between the data and the simulation with the protrusion is the quick depletion from the helper gate. This is discussed in section 3.1. These gate-gate maps are not in complete agreement with each-other. The helper gate depletes too quickly, and the QPC gate does not pinch off quickly enough.

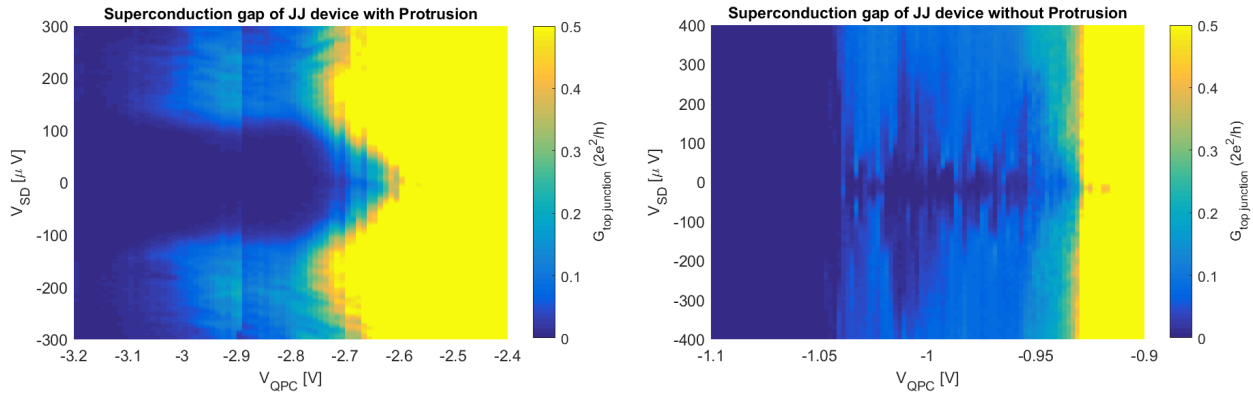

Figure 3.9: Conductance map as a function of V_{QPC} and V_{SD} for the Josephson junction device with protrusion(left) and without protrusion(right). For the left we see a clear superconducting gap, and for the right we do not see any hard gap

In the measured data for the Josephson junction device without the protrusion, we see that pinch-off occurs for the helper gate at $V_{helper} = -0.8V$ (figure 3.7, right), whereas in our simulations we see the same pinch-off at $V_{helper} = -0.45V$ (figure 3.8, right). This trend also occurs in the NIS simulations, and we believe it is caused by the helper gate depleting the area near it too quickly. For the same device we also see that for $V_{helper} = 0V$, we have that the measured pinch-off occurs at $V_{QPC} = -0.9V$, whilst our simulations predict a value of $V_{QPC} = -1.2V$. Our interpretation of this behavior is that depletion in the 2DEG happens more locally in the area below the gates than what we would expect, as we also saw in the pinch-off data. This seems to be reoccurring phenomenon in our model, as the gate-gate maps for the NIS device had the same features. This is not detrimental to the results, since the qualitative nature of the electrostatics are present in our simulations. This discrepancy could likely be solved by more extensive tweaking of the model parameters.

For the device with the protrusion, we see that for $V_{QPC} = 0V$, the simulated device shows the same features as the device without the protrusion, in terms of the helper gate depleting too quickly. The

real device pinches off at $V_{helper} = -0.8V$, whilst our simulations pinches off at $V_{helper} = -0.45V$. We see that the simulated device have a pinch-off for $V_{helper} = 0V$, $V_{QPC} = -2.5V$, and we have the same case for the real device (This is caused by our fitting of V_0, if it did not pinch off at the same value, we would redo the fitting process).

In the experimental data from the JJ device seen in figure 3.7, a "tail" of weak conductance is visible from $V_{helper} = 0V.. - 0.4V$. We believe that this tail is caused by the protrusion on the helper gate. This is supported by the gate-gate maps from the NIS QPC device experimental data, seen in figure 3.14. From the JJ device data, it is clear that the conductance tail is caused by the protrusion. For the NIS QPC device, we have virtually removed the protrusion and simulated the results. This is shown in figure 3.15.
In figure 3.9 we see the experimental data that suggest that the protrusion provides better spectroscopy. It is clear that for the device with the protrusion, there is a well defined conductance gap in the region of $|V_{SD}| = 100\mu V$, that is not present in the data from the device without the protrusion.

3.2.2 Normal-Insulator-Superconductor Devices

In the following section, we show 2D density maps in the 2DEG plane. Figures 3.10, 3.11 and 3.12 show the maps for the NIS Devices

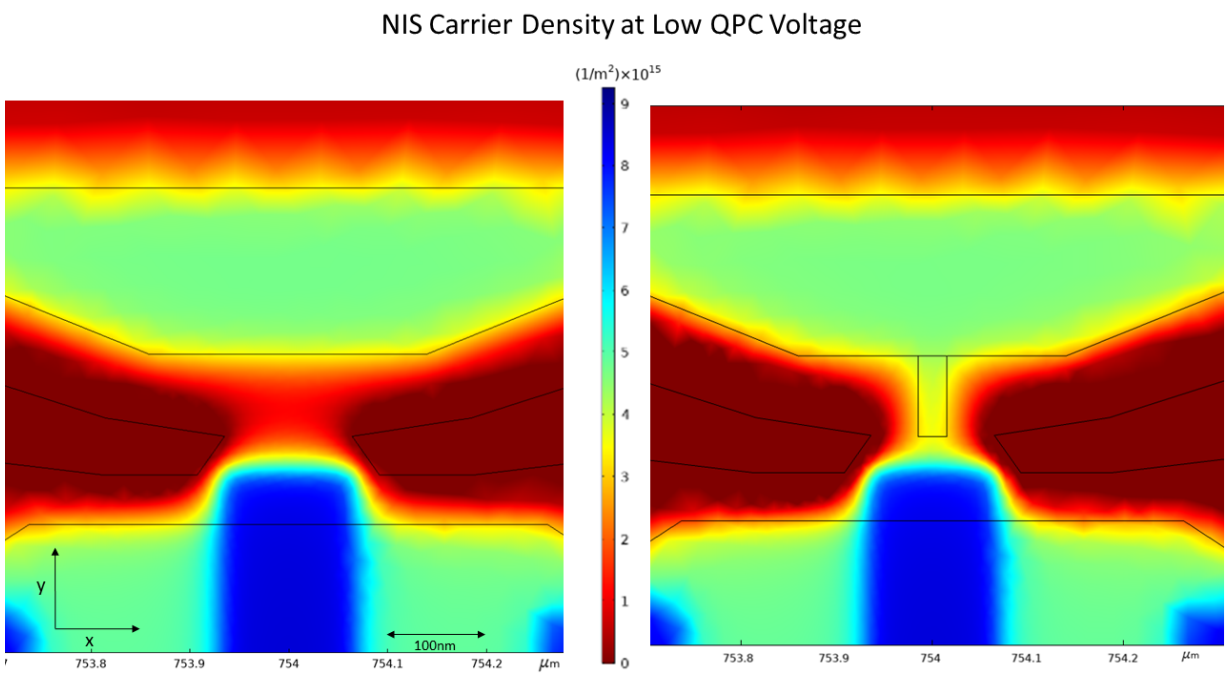

Figure 3.10: 2D maps of electron density at the surface of the 2DEG. For the left we have the device without the protrusion, and for the right we have the device with the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = -0.42V$ for the right figure, and $V_{helper} = 0V$ and $V_{QPC} = -0.32$ for the left figure. We consider this a low QPC voltage for both devices, in relation to the pinch off voltage

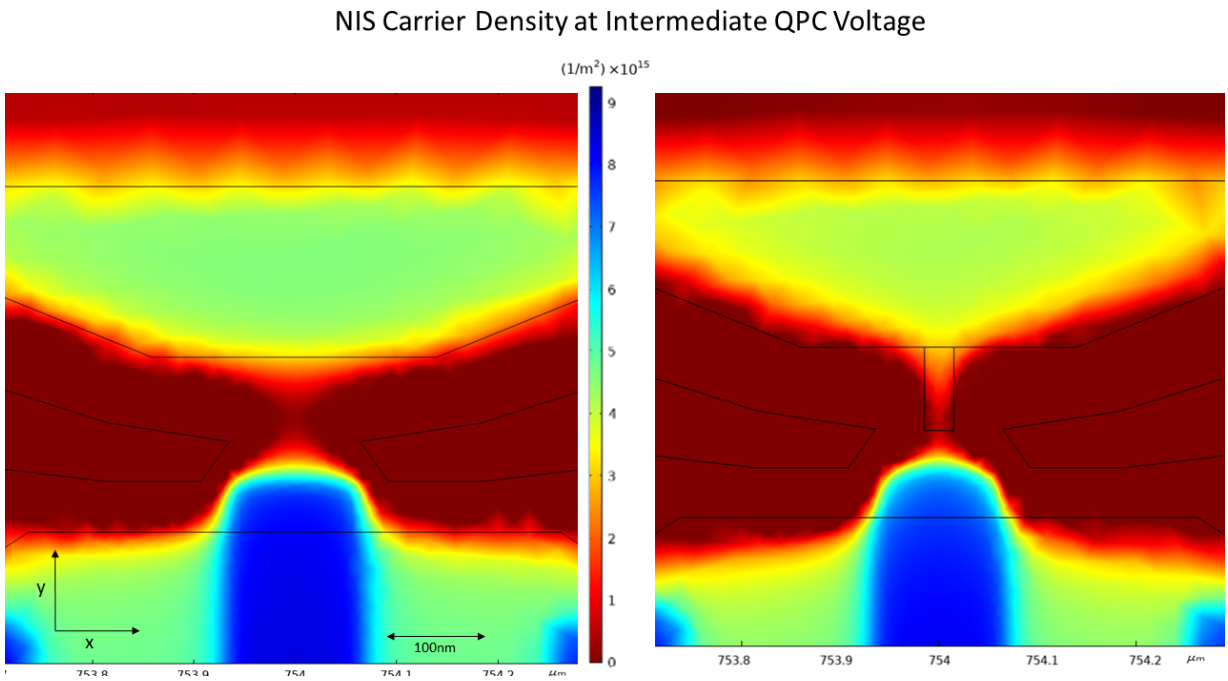

Figure 3.11: 2D maps of electron density at the surface of the 2DEG. For the left we have the device without the protrusion, and for the right we have the device with the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = -1.38V$ for the right figure, and $V_{helper} = 0V$ and $V_{QPC} = -0.64V$ for the left figure. We consider this a intermediate QPC voltage for both devices, in relation to the pinch off voltage

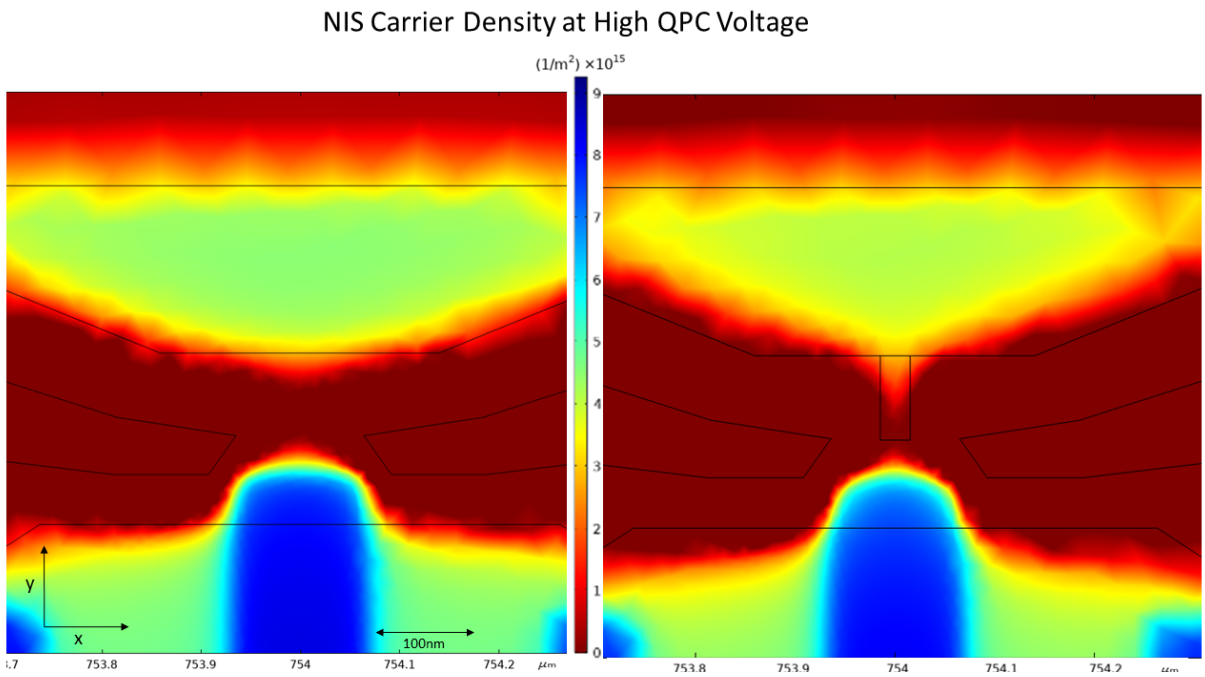

Figure 3.12: 2D maps of electron density at the surface of the 2DEG. For the left we have the device without the protrusion, and for the right we have the device with the protrusion. This map is for values of $V_{helper} = 0V$ and $V_{QPC} = -1.49V$ for the right figure, and $V_{helper} = 0V$ and $V_{QPC} = -0.69V$ for the left figure. We consider this a high QPC voltage for both devices, in relation to the pinch off voltage

For the NIS device with all gates at $0V$, see figure 3.10, we see the same behavior as we saw in

the Josephson junction device. As we increase the QPC voltage to near pinch-off, see figure 3.11, the device with the protrusion has a narrow area of relativity high density in the middle of the QPC channel, that is not present without the protrusion. We interpret this as the protrusion facilitating a sharper and smaller potential barrier.

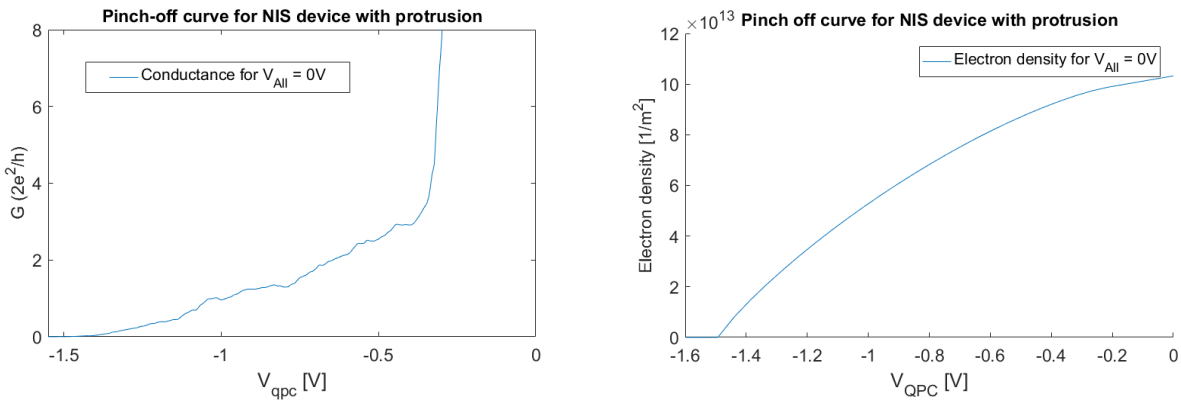

Figure 3.13: Pinch-off plot for the NIS device. The left figure is the measured conductance, while the right figure is the simulated electron density It shows complete pinch off at $V_{QPC} = -1.5V$ for both cases

The calculated pinch-off plots for the NIS device with the protrusion agree well with, as seen in figure 3.13. Experimental pinch-off happens at $V_{QPC} = -1.5V$ and our simulations pinch off at $V_{QPC} = -1.5V$.

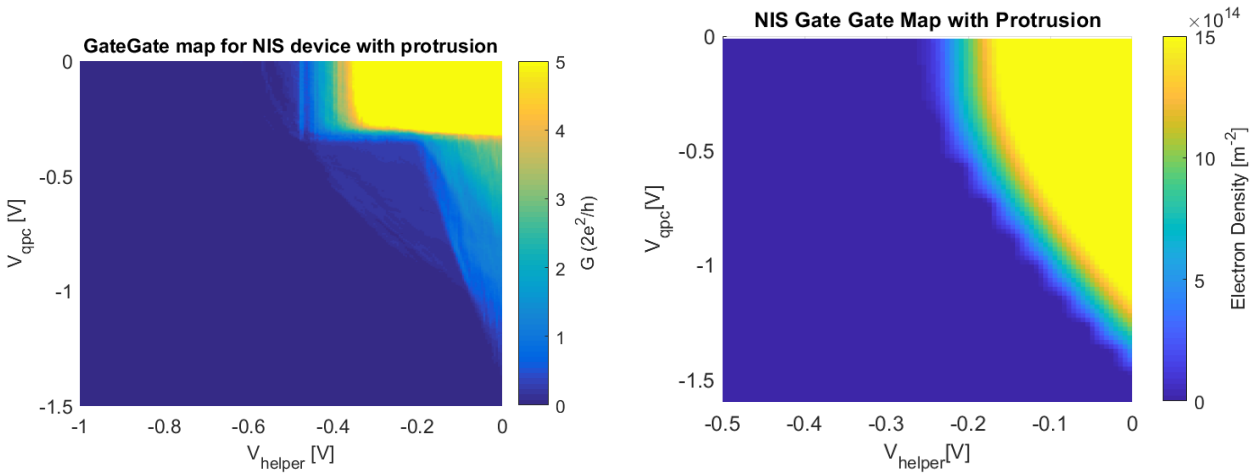

Figure 3.14: Gate-gate map for the NIS QPC experimental data (left) and simulated (right).

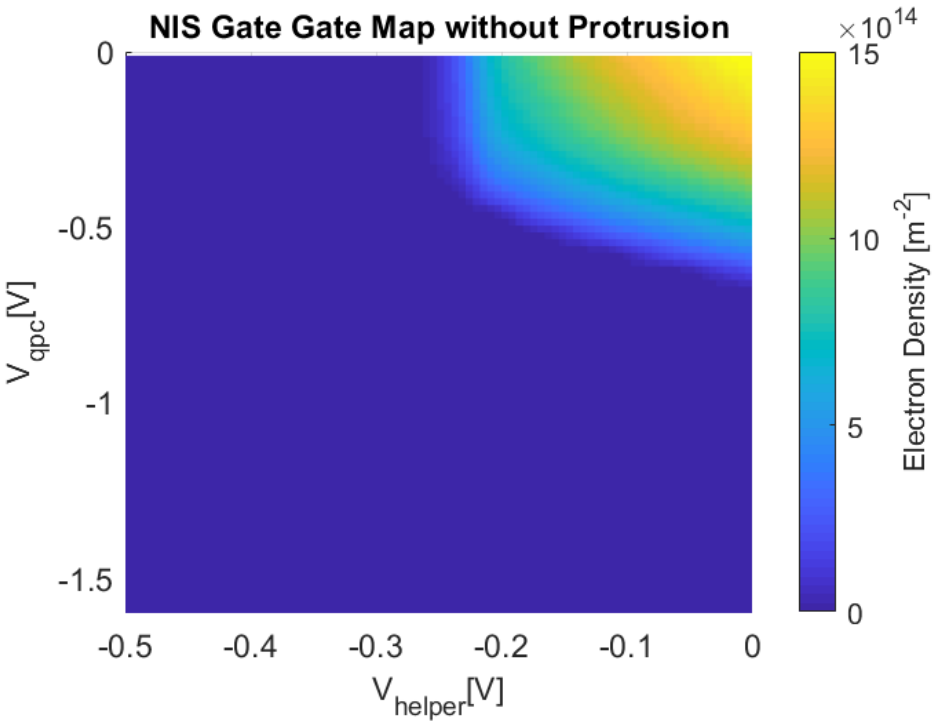

Figure 3.15: NIS QPC gate-gate map without protrusion. The density is compared to the device with protrusion (see figure 3.14), this is caused by our measuring method (see section 3.1).

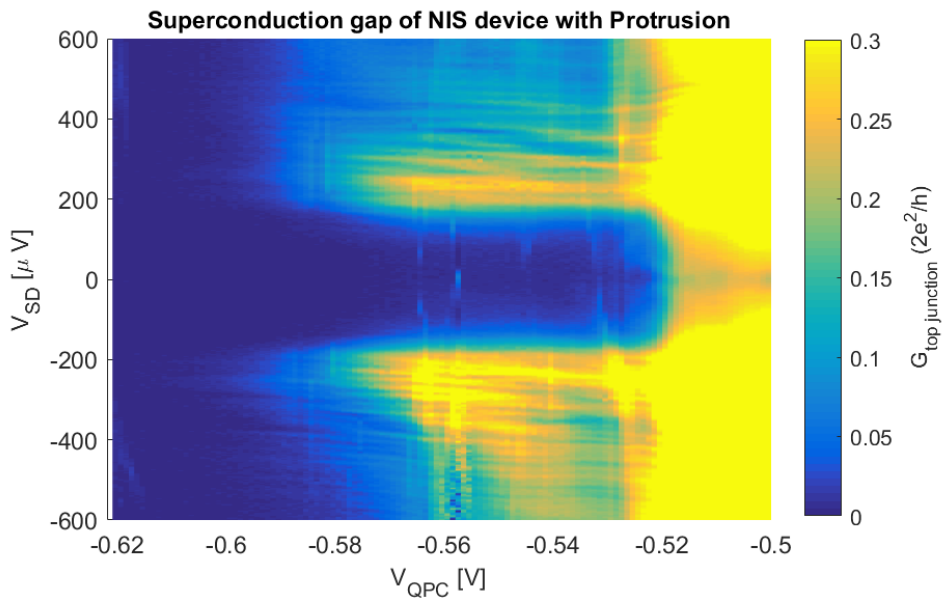

Figure 3.16: Conductance map of NIS device with protrusion, as a function of V_{QPC} and V_{SD}. For this device we see a clear superconducting gap, just as we saw figure 3.9 (left).

From figure3.16 and 3.9(left) we see that the devices with the protrusion have a well defined superconducting gap, where as seen in 3.9(right) we have no clear superconducting gap.

We can now compare the NIS Device simulation gate-gate maps with the gate-gate map from the experiment shown in figure 3.15 and figure 3.14. The first thing to notice is that the helper gate pinches off a lot earlier in our simulations, at low V_{QPC}. The helper gate in the experiment pinches off at around $V_{helper} = -0.4V$, whilst our simulation pinches off at around $V_{helper} = -0.2V$. We believe

that this happens in our simulation partly because of V_0. in practice, V_0 acts like a depletion point, which means that the area below the gates will deplete quickly when $eV_{pot} \approx V_0$. The pinch-off behavior in the range $V_{QPC} = 0V... - 1.5V$, $V_{helper} = 0V... - 0.2V$ is well captured by our simulation, having the same shape as the experiment.

The gate-gate map without the protrusion also shows what we would expect, given the data from the Josephson junction device (figure 3.7), the QPC gate causes pinch-off at lower voltages ($V_{helper} = -0.6V$ in figure 3.15, right), and the overall shape of the gate-gate map forms a rectangle and missing its "tail". We do not have any experimental data to compare this specific gate-gate map to, but the simulation has the square-like shape as expected.

In figure 3.16, we see the same clear superconducting gap for the NIS QPC device with the protrusion, as we saw in the JJ Device with the protrusion (figure 3.9). There is not any experimental data from the NIS device without a protrusion, however we can see that both the NIS and JJ devices with a protrusion have a clear superconducting gap (see figure 3.16 and figure 3.9). The data from the JJ device without the protrusion does not show a clear superconducting gap. The devices with a protrusion also share a common feature, a sharp and narrow density channel in the middle of the QPC (figure 3.3 and 3.11). This feature is not present in any of the devices without a protrusion, we instead observe a broad density channel between the helper gate and the wire. This gives us reason to believe that a sharp and narrow density channel near the QPC is consistent with a clear superconducting gap.

CHAPTER 4

Conclusions

We have conducted electrostatic simulations of four separate device geometries, and compared our simulations with experimental data when available. We found that our model reproduces qualitatively the experimental features of the measured conductance, but lacks quantitative accuracy in its current state.

We have reproduced pinch-off plots and gate-gate maps for the Josephson junction device and the NIS QPC device, with protrusions, that show pinch off for the same QPC gate voltages as the experimental data. For the Josephson junction device, we reproduced pinch off at $V_{QPC} = -2.5V$ (figure 3.5) and for the NIS QPC device we reproduced pinch-off at $V_{QPC} = -1.5V$ (figure 3.13). For the Josephson Junction device without the protrusion, our simulations pinched-off at $V_{QPC} = -1.2V$, whilst the experimental data showed pinch-off at $V_{QPC} = -0.9V$ (figure 3.6). Further work could aim to improve this model by extensive parameter tweaking, or expanding the model to make simulations of conductance.

We also report that our simulations agree with experimental intuition regarding the use of a protrusion on the helper gate of the devices. Our simulations produce 2D maps of the electron density in the two dimensional electron gas, that shows a sharper tunneling barrier between the two electron reservoirs, compared to the devices that lack the protrusion on the helper gate. (figures 3.2, 3.3, and 3.4). This has been experimentally employed to obtain high resolution tunneling spectroscopy of the density of states of states at the boundaries of the superconducting regions of the devices [Fornieri et al., 2019]

Future improvements of the model could lead to improvements and designs of more sophisticated devices, which could become the building block for a topological quantum computation [Karzig et al., 2017].

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Appendices

APPENDIX A

Theory

A.1 Finite Element Method

COMSOL uses the Finite Element Method (FEM) to numerically solve the Poisson equation for the given model. This is done by converting the problem into its weak form (eq. A.3), and solving it using the FEM [COMSOL, 2017]. The following is a brief explanation on how this works.
First, let us consider a general Poisson equation

$$-\nabla^2 u = f \quad in\, \Omega \tag{A.1}$$

Where Ω is the domain we wish to simulate. Then we wish to convert this equation into its weak form. This is done by multiplying with a arbitrary test function v and integrating over the domain. This gives us the following.

$$\int_\Omega -\nabla^2 uv \, \mathrm{d}x = \int_\Omega fv \, \mathrm{d}x \tag{A.2}$$

Then using Green´s identities and integration by parts, we find the following.

$$\int_\Omega fv \, \mathrm{d}x = \int_\Omega \nabla u \cdot \nabla v \, \mathrm{d}x = \phi(u,v) \tag{A.3}$$

Then we define $F(v) = \int_\Omega fv \, \mathrm{d}x$. Now we wish to find a $u \in V$ such $F(v) = \phi(u,v) \;\; for\, all\, v \in V$ where V is a Hilbert space. It can be rather difficult to find solutions for u that holds true for all v over the entire domain. Therefore we split the problem into a finite number of sub-spaces of V, so we have $V^h \subset V$, and instead solve the variation problem for each sub space. This implies that the approximate solution is expressed as a linear combination of a set of basis function that belong to the subspace. In COMSOL this is done by dividing the entire domain into smaller sub domains called elements. Elements are bounded by points called nodes, and each node has a set of basis functions. Choosing these basis functions for the subspace, we have a set of n number of equations and unknown variables, where n is the dimension of V^h.

By imposing the boundary conditions and then solving these set of equations, we find approximate solutions within the element. These solutions have to comply with continuity conditions with the next element, at the nodes or edges of the element. Solving each element we find the solution for the entire domain. The size of the mesh (the assembly of elements), can be adjusted to the chosen geometry for the model. A finer mesh means that the solution should be more accurate, at the cost of computing speed. In order to avoid high computing time, we have defined a domain within our geometry where the mesh is very fine, an area we are specifically interested in, whilst the mesh outside of this domain is a lot coarser.